EE105 – Fall 2015
Microelectronic Devices and Circuits
Multi-Stage Amplifiers

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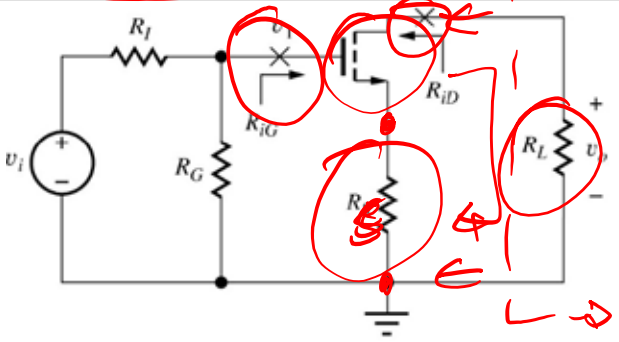
Terminal Gain and I/O Resistances of MOS Amplifiers

Common Source (CS)



(a)

$$A_{V,t} = -\frac{g_m R_L}{1 + g_m R_S}$$

$$R_i = \infty$$

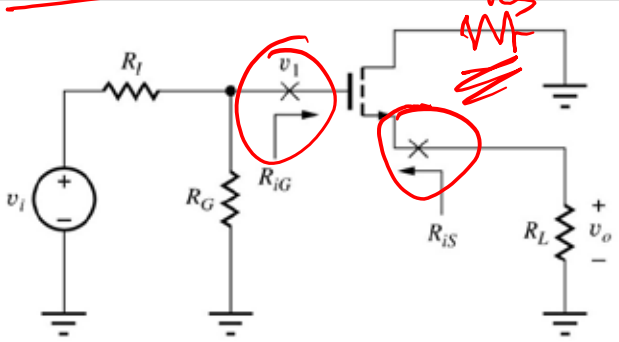
$$R_o = \left[r_o\left(1 + g_m R_S\right)\right]$$

$$A_{I,t} = \infty$$

Without degeneration:

Simply set $R_S = 0$

Common Drain (CD)



(b)

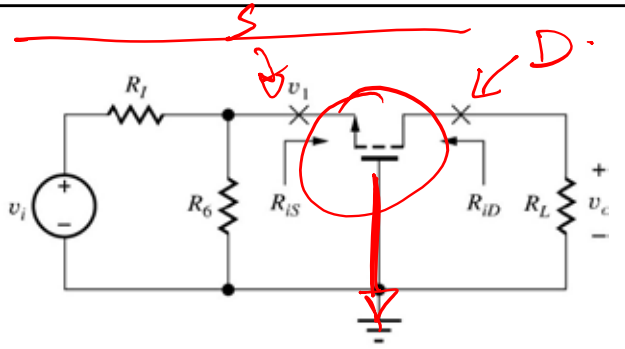
$$A_{V,t} = \frac{R_L}{\frac{1}{g_m} + R_L}$$

$$R_i = \infty$$

$$R_o = \frac{1}{g_m}$$

$$A_{I,t} = \infty$$

Common Gate (CG)



(c)

$$A_{V,t} = g_m R_L$$

$$R_i = \frac{1}{g_m}$$

$$R_o = \left[r_o\left(1 + g_m R_E\right)\right]$$

$$A_{I,t} \approx 1$$

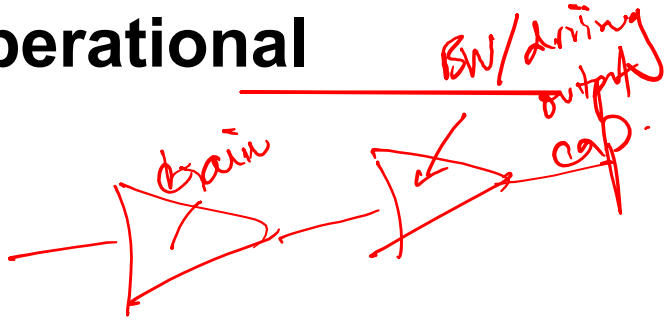
For the gain, R_i, R_o of the whole amplifier, you need to include voltage/current dividers at input and output stages

Summary of MOS Single-Transistor Amplifiers

MOS	Common Source	Common Source with Deg.	Common Drain	Common Gate
R_i	∞	∞	∞	Small
R_o	Large	Very Large	Small	Large
A_V	Moderate	Small	~ 1	Moderate
f_H	Small	Moderate	Large	Large

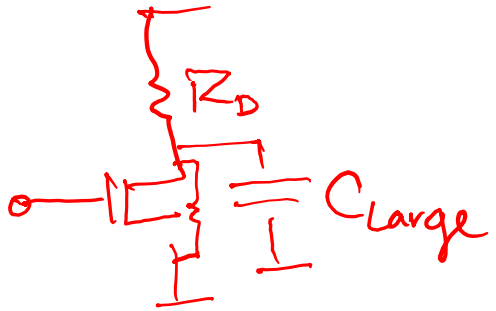
Single Stage Amplifier Cannot Meet All Requirements

- For example, a general purpose operational amplifier requires
  - High input resistance ~ 1MΩ
  - Low output resistance ~ 100Ω
  - High voltage gain ~ 100,000



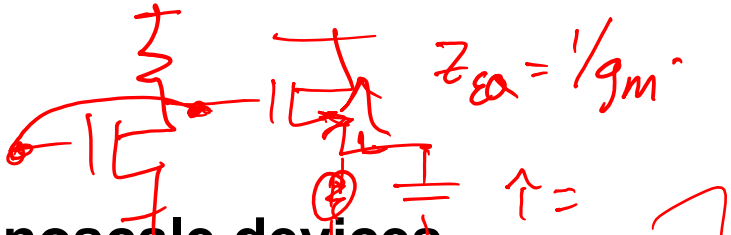
- No single transistor amplifier can satisfy all spec's
- Cascading multiple stages of amplifiers offers a path towards the design

Multistage Amplifiers



$\tau = C_{large}(R_D \| r_o)$

- **Usually**
  - **An input stage to provide required input resistance**
  - **Middle stage(s) to provide gain**
  - **An output stage to provide required output resistance or drive external loads**



- **More gain !**
  - **Gain/stage limited, especially in nanoscale devices**

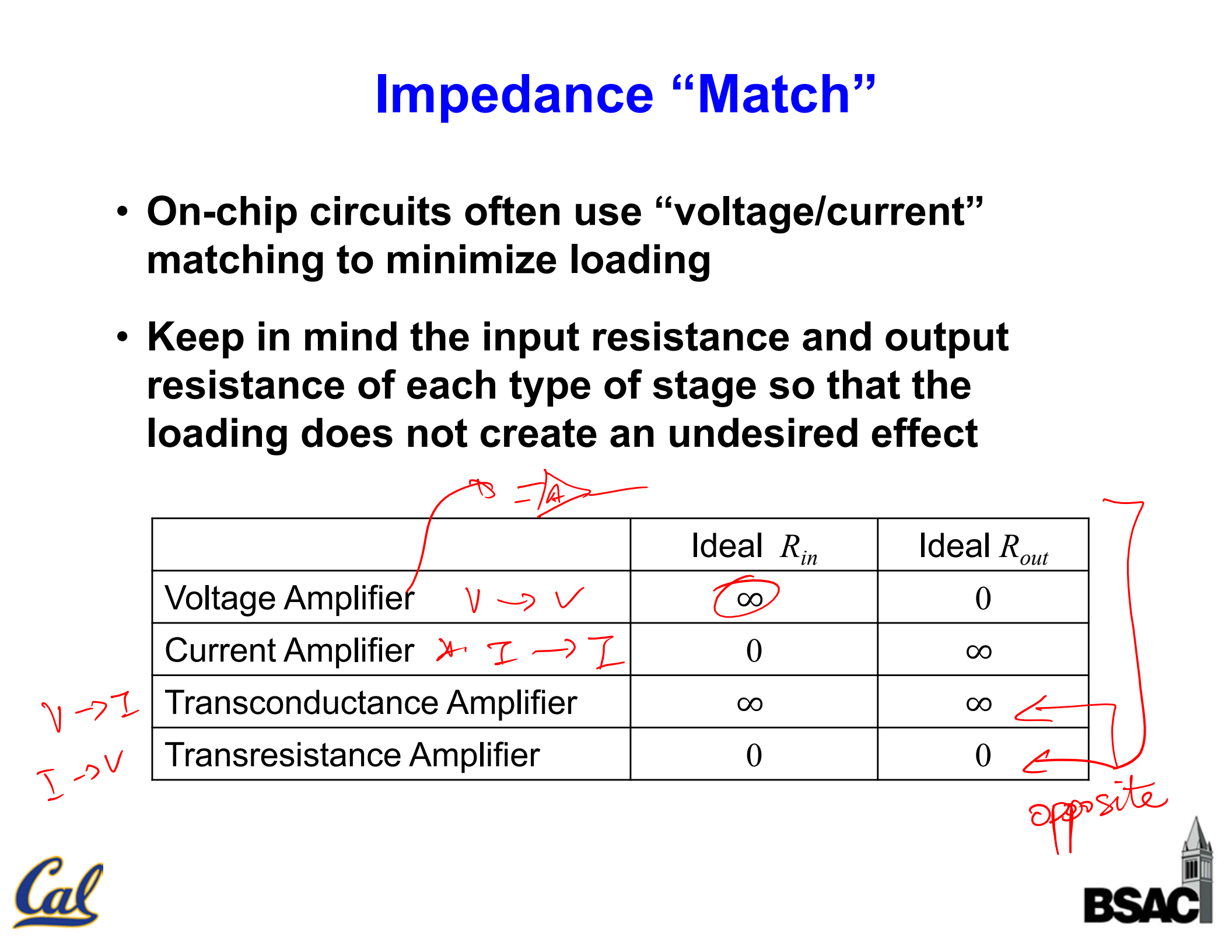
$\tau = C_{large}(1/g_m)$

- **Improve Bandwidth**
  - **De-couple high impedance nodes from large capacitors**
- **DC coupling (no passive elements to block the signal)**
  - **Use amplifiers to naturally "level shift" signal**

Impedance "Match"

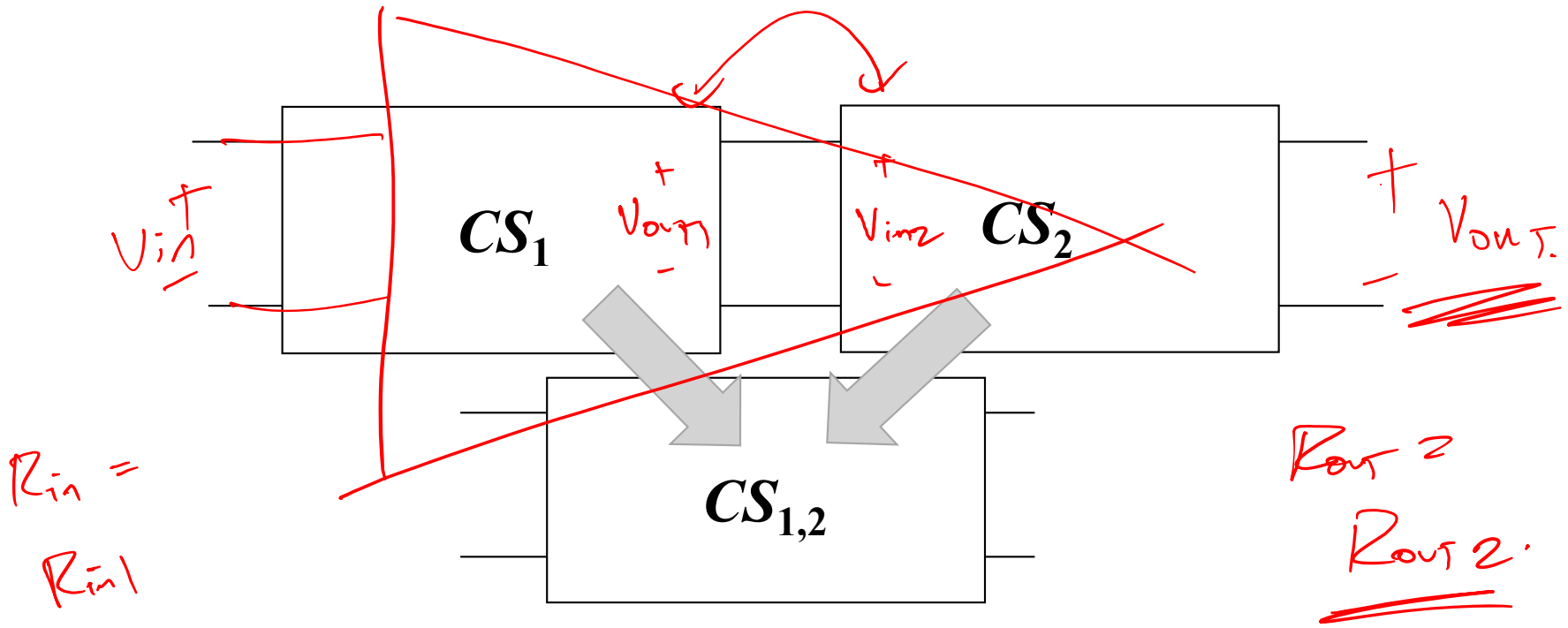
- **On-chip circuits often use "voltage/current" matching to minimize loading**
- **Keep in mind the input resistance and output resistance of each type of stage so that the loading does not create an undesired effect**

	Ideal R_{in}	Ideal R_{out}
Voltage Amplifier	∞	0
Current Amplifier	0	∞
Transconductance Amplifier	∞	∞
Transresistance Amplifier	0	0



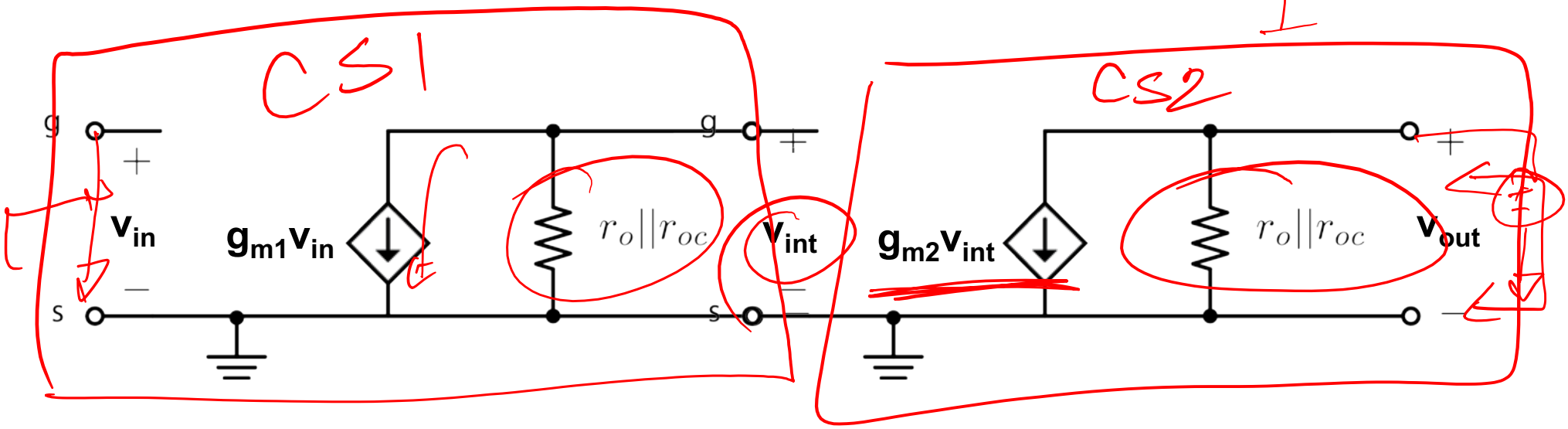
Two-Stage Voltage Amplifier

- **Boost gain by cascading Common-Source stages**



Can combine into a single 2-port model
Results of new 2-port: $R_{in} = R_{in1}$, $R_{out} = R_{out2}$

CS Cascade Analysis



Results of new 2-port:

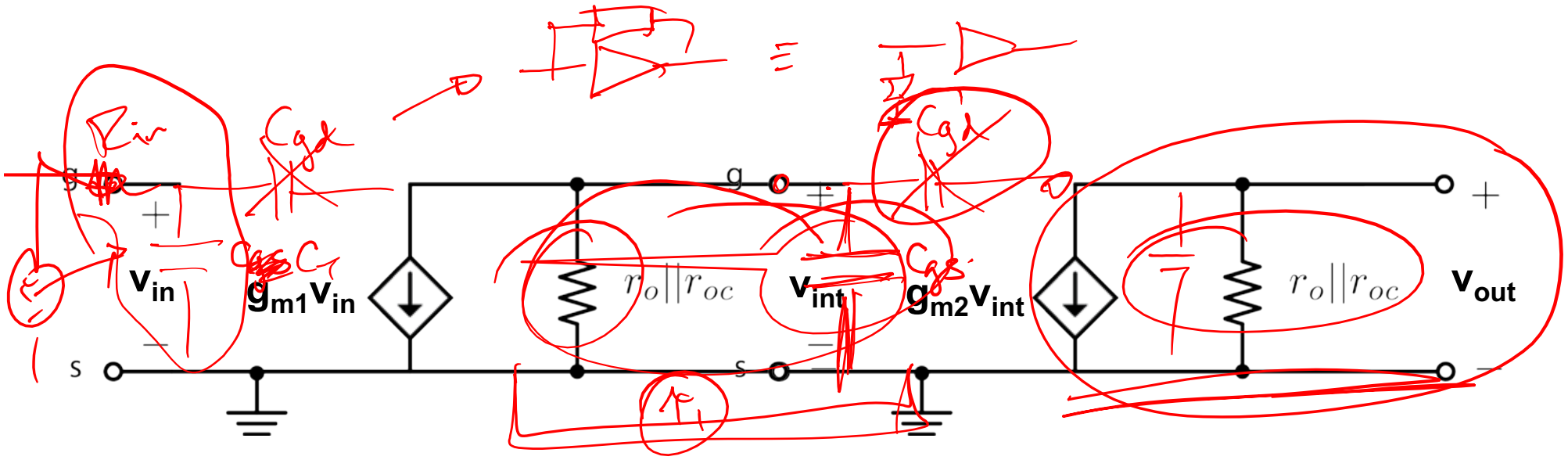
$R_{in} = R_{in1} =$ ∞

$R_{out} = R_{out2} =$ $r_o || r_{oc}$

$A_V = v_{out}/v_{in} =$ $\frac{v_{int}}{v_{in}} \cdot \frac{v_{out}}{v_{int}} = (-g_{m1} \cdot (r_o||r_{oc})) \cdot (-g_{m2} \cdot (r_o||r_{oc}))$

$= g_{m1} g_{m2} (r_o||r_{oc})^2$

CS Cascade Bandwidth



$$C_M = C_{gd}(1-A), \quad A = -g_m(r_o||r_{oc})$$

$$C_T = C_{gs} + C_M$$

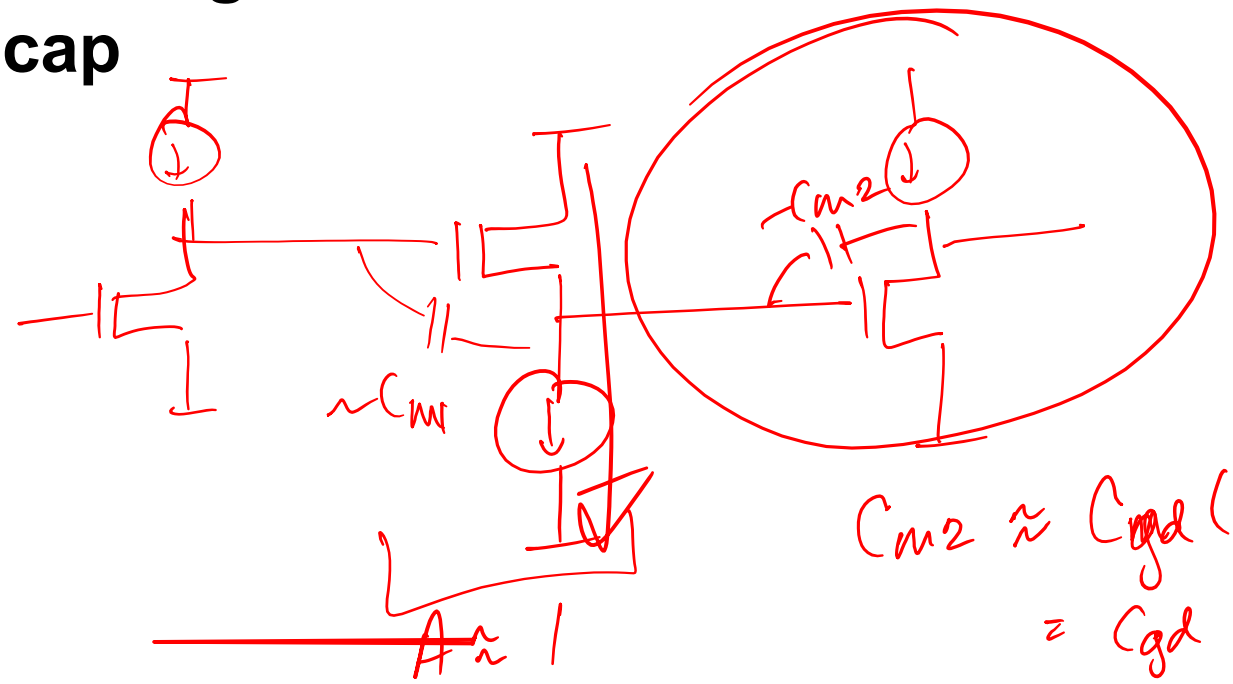
Two time constants:

$\tau_1 = (C_{gs} + C_M) \cdot (r_o||r_{oc})$

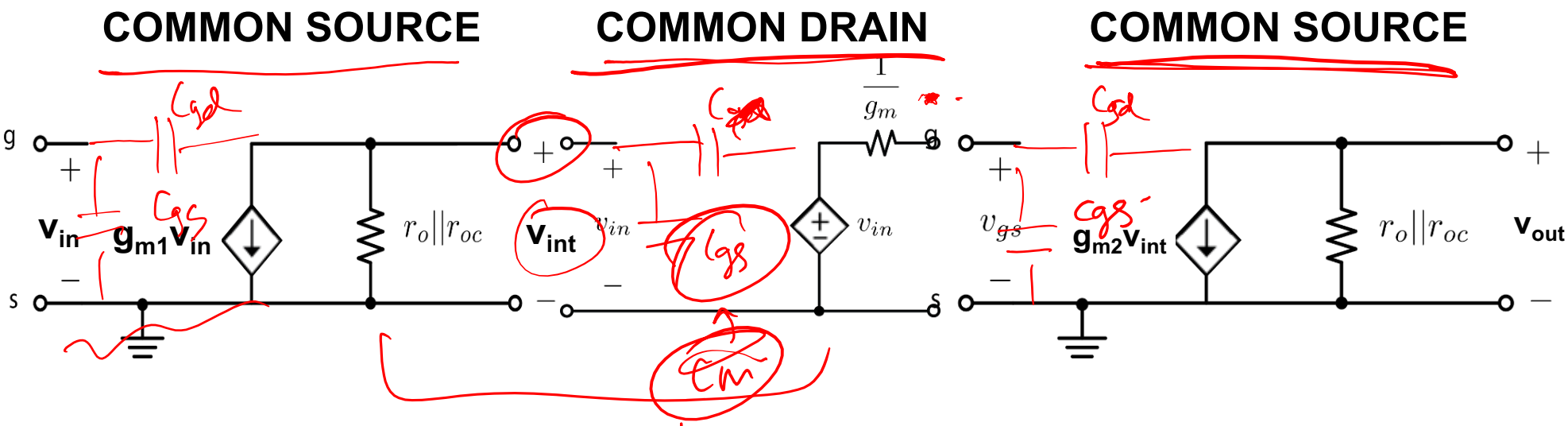
$\tau_2 =$

Bandwidth Extension

- Common Source stage has high gain, but low bandwidth
- Note that Miller effect is the culprit
- Follower stage can buffer source resistance from Miller cap



Bandwidth Extension Using Source Follower (SF)



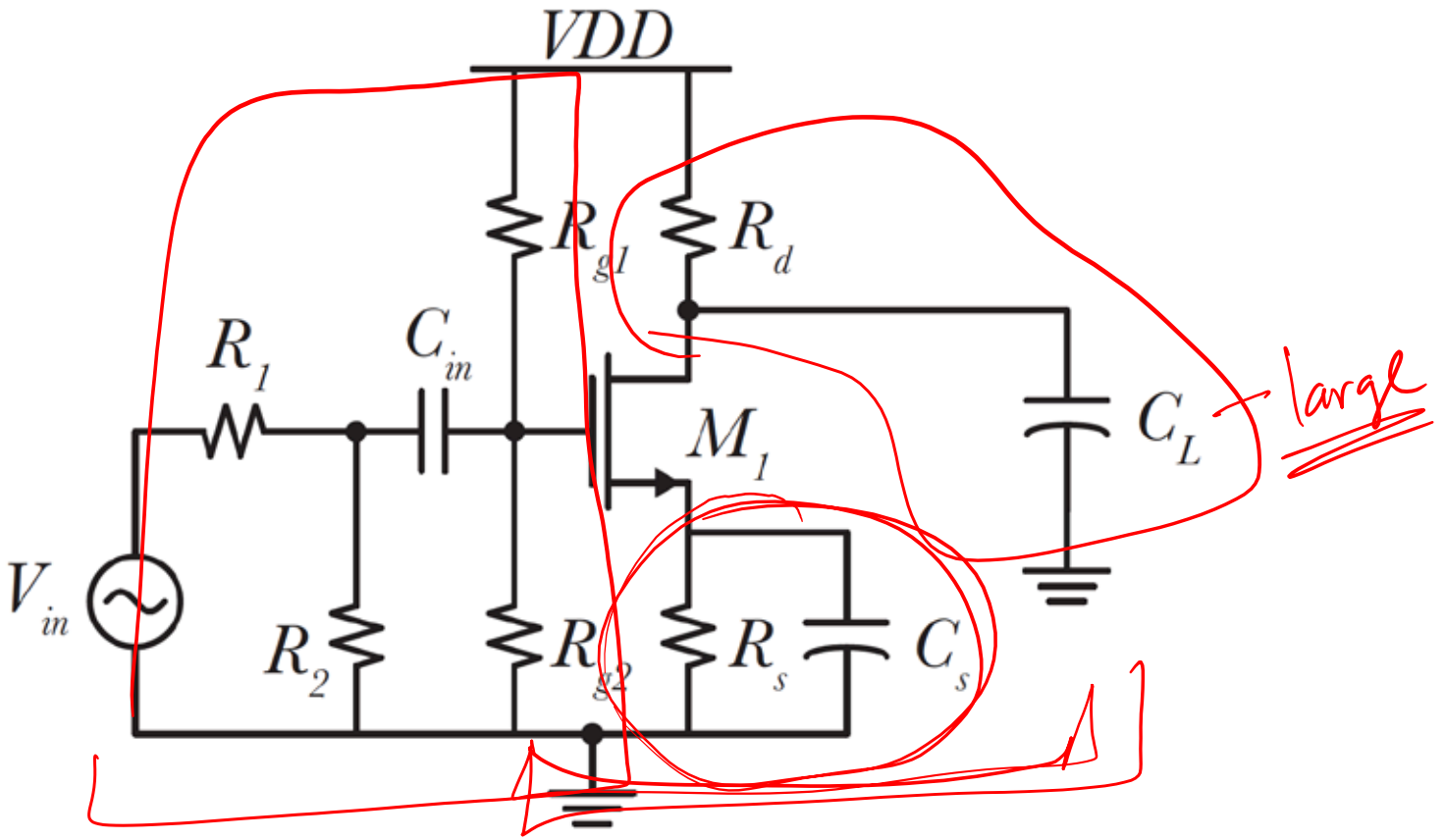
$$\frac{V_{out}}{V_{in}} = \frac{V_{int}}{V_{in}} \cdot \frac{V_{int2}}{V_{int}} \cdot \frac{V_{out}}{V_{int2}} = -g_{m1}(r_o||r_{oc}) \cdot 1 \cdot g_{m2}(r_o||r_{oc})$$

$$= g_{m1}g_{m2}(r_o||r_{oc})^2 \quad \text{← unchanged.}$$

$$\tau_1 = (r_o||r_{oc}) \cdot (C_{gs} + C_m)$$

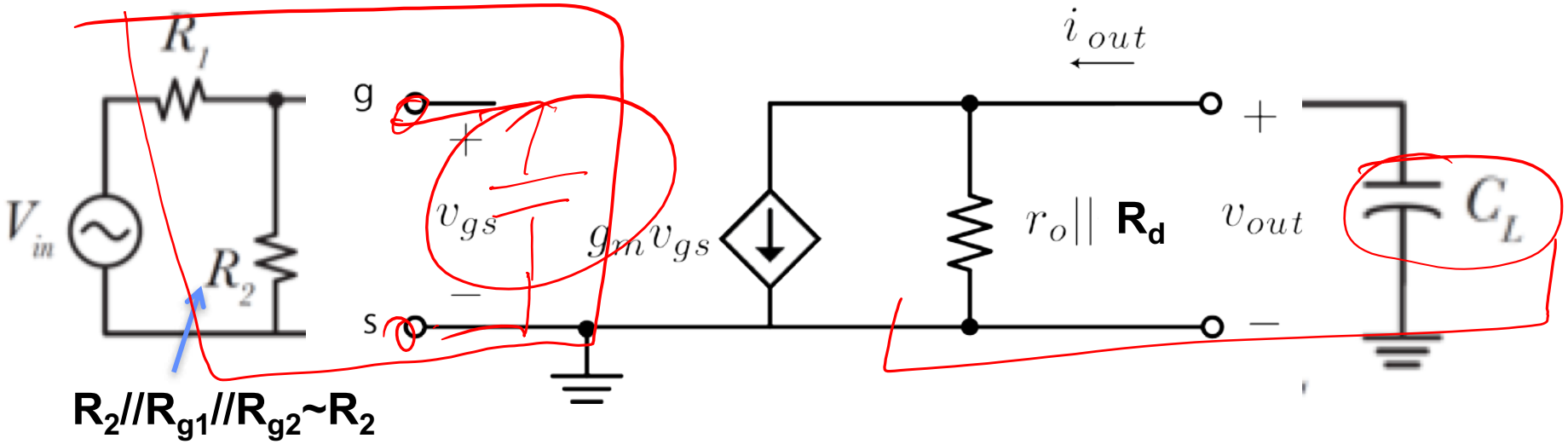
$$\tau_2 = \frac{1}{g_m}\left(C_{gs} + \frac{C_{gd}(1 + g_{m2}(r_o||r_{oc}))}{C_m}\right)$$

CS Example with Cap Load



- C_{in} and C_S are very large, therefore they look like short circuits to the AC signal.
- If C_L is very large, its pole dominates, let's analyze

CS with Cap Load – Small Signal

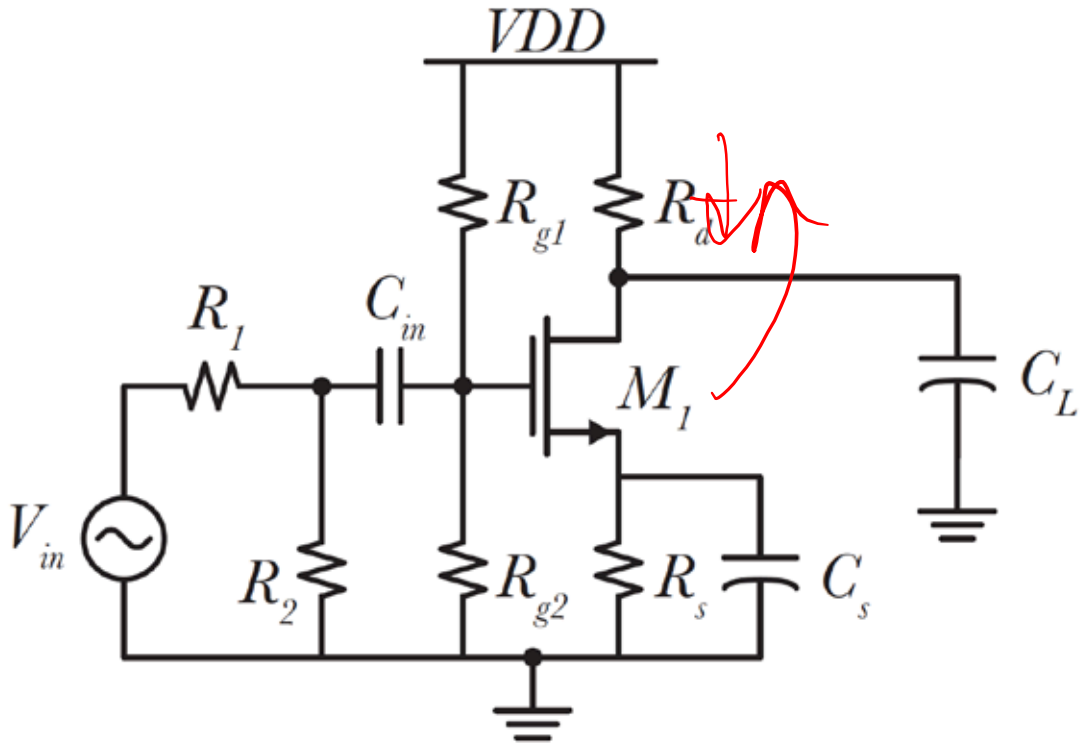


$R_2 // R_{g1} // R_{g2} \sim R_2$

$\tau_1 = (R_1 // R_2)(C_{gs} + C_M)$ $\quad \tau_2 = C_L \cdot (r_o || R_D)$

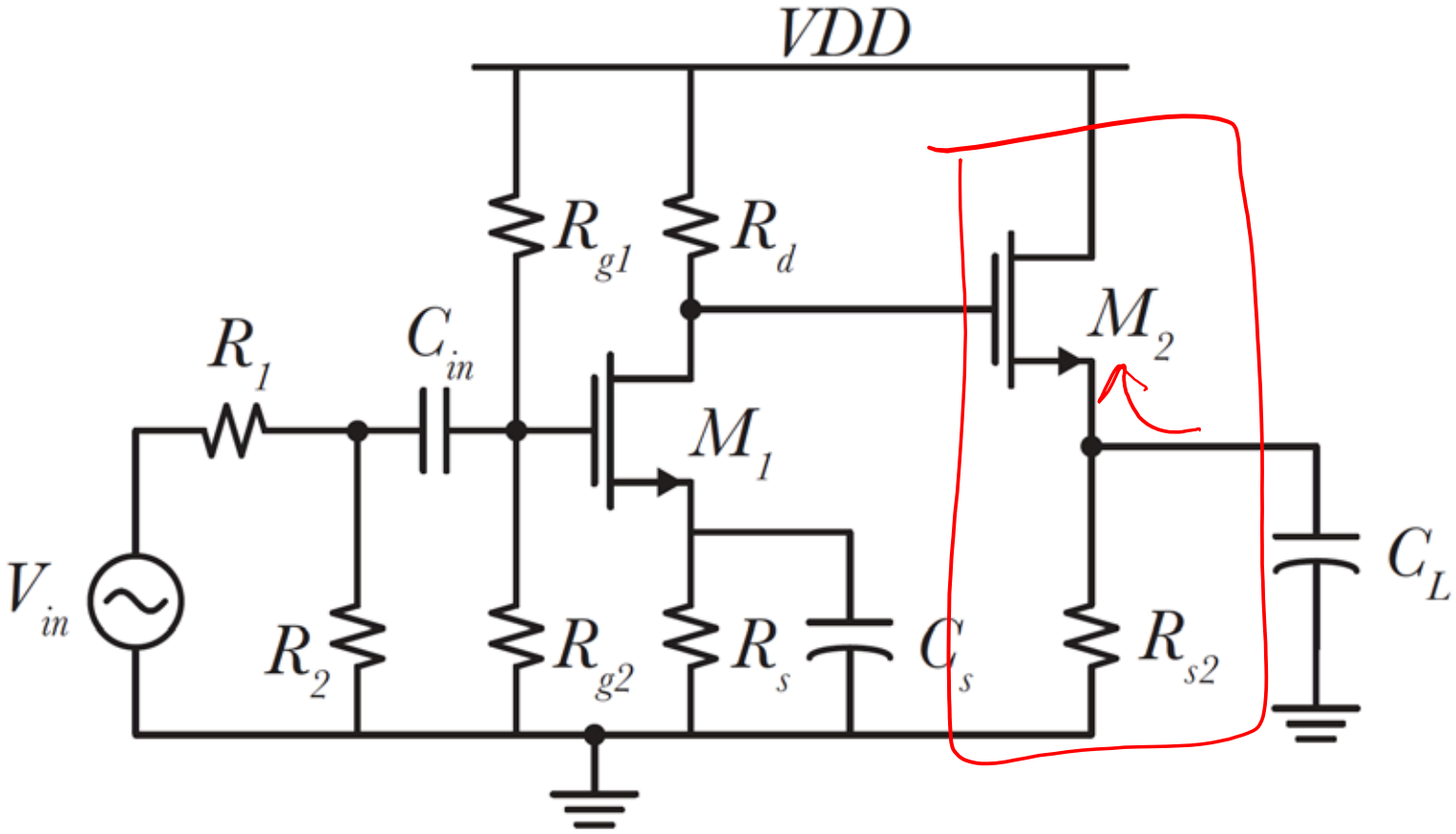
- What are the time constants associated with the capacitors in this circuit?
- What can we do if we have to drive a large C_L?

CS with Cap Load – Bandwidth



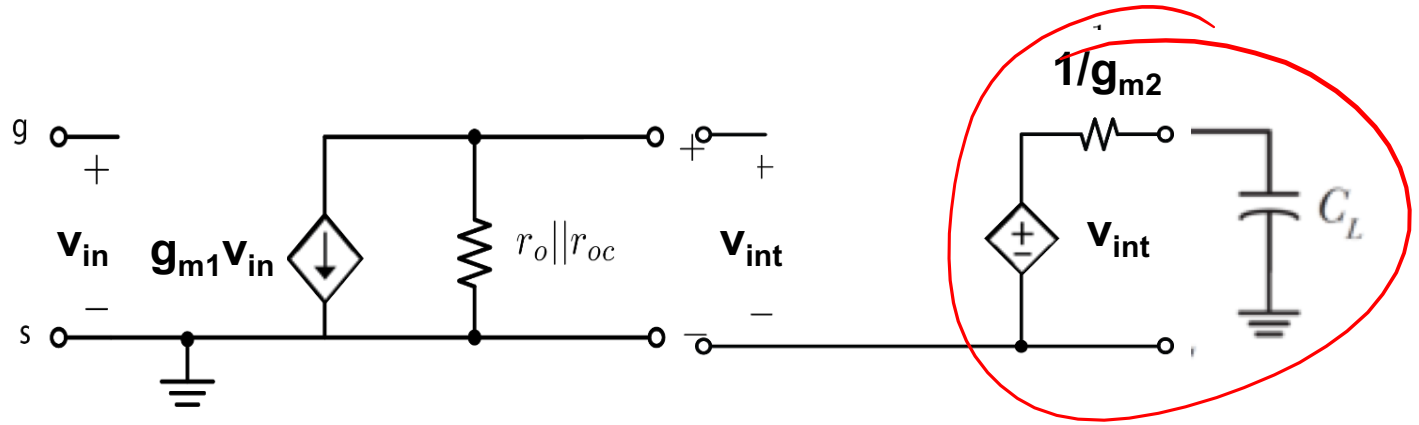
- How can we reduce the impact of C_L?
- One way is to reduce the resistance R_d, but this reduces our low-frequency gain
- To recover the gain we can increase g_{m1}. *What does this cost us?*

CS with Cap Load – BW Extension



- A better way to extend the bandwidth is to add a source-follower stage.
- Similar to previous example

CS with Cap Load – BW Extension

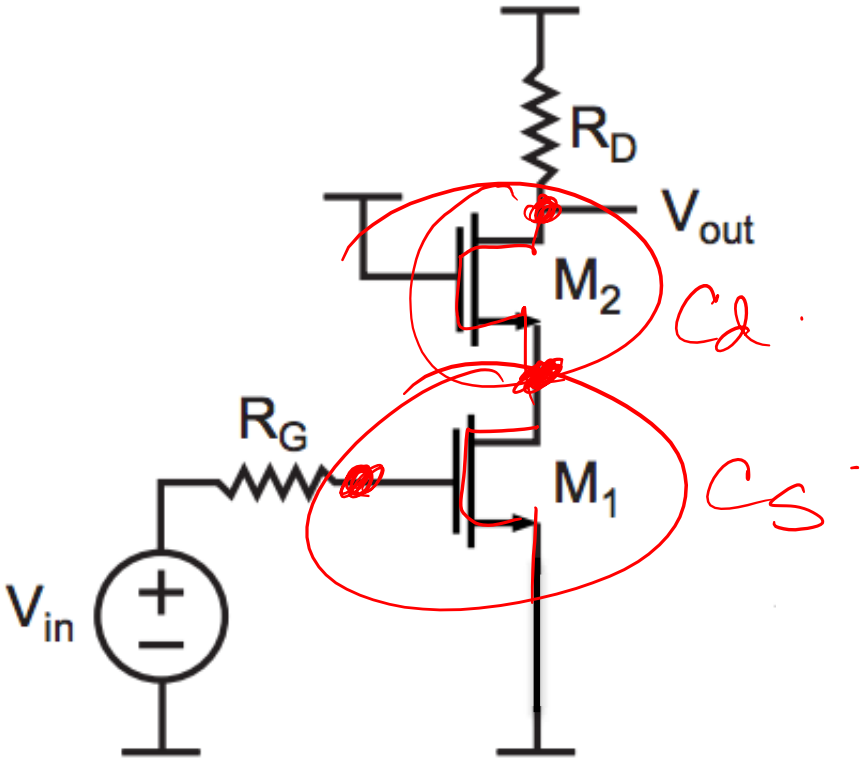


$$\tau_2 = C_L \cdot \frac{1}{g_{m2}}$$

- By adding a CD (Source Follower) we can increase the bandwidth
- It costs us power for the CD stage
- Remember that increasing the BW by increasing g_{m1} costs us much more

CS + CG ≈ Cascode

- **Common source provides gain, CG acts as a buffer, but is it even helping?**
- **How do you bias this circuit?**



High R_{OUT}.

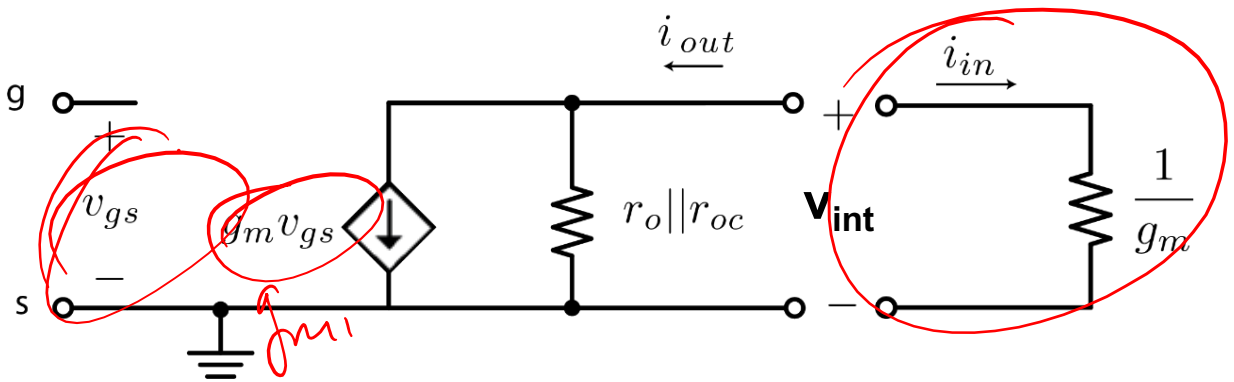
Headroom problems.

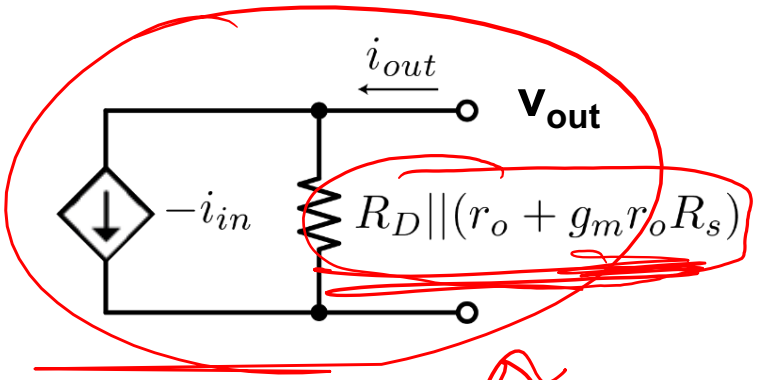
CD.

CS.

Merged CS + CG = Cascode

- Let's apply 2-port small-signal analysis



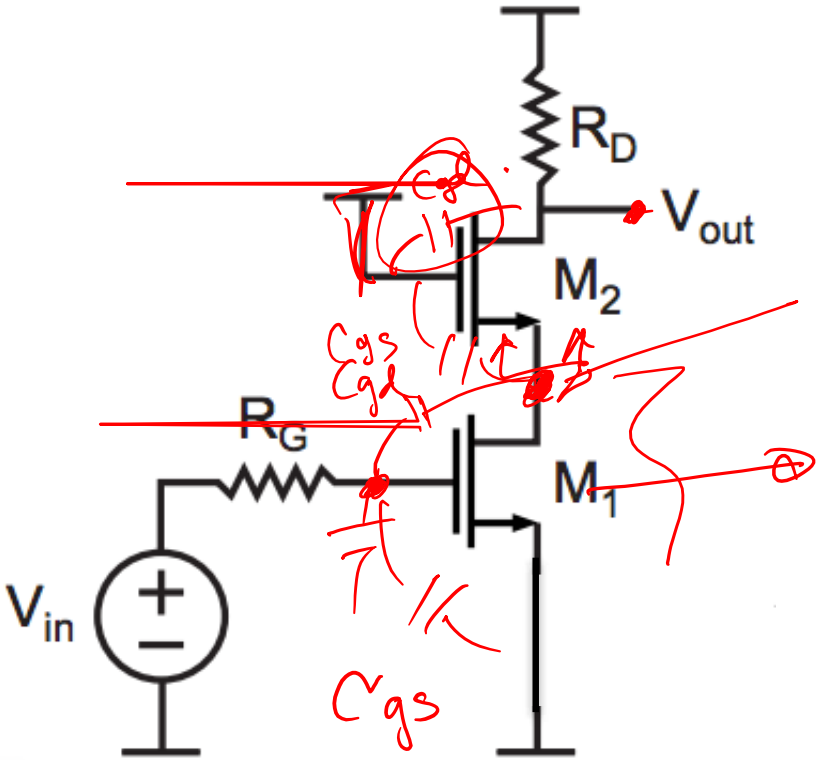


$g_{m1} \cdot \left(R_D \,||\, (r_o + g_{m2} r_o R_S) \right)$

- In this case, we care about the *input current* to the second stage
- Note that the input resistance of the CG is low, therefore the majority of the CS current is fed to the CG
- $A_v = \frac{V_{out}}{V_{in}} = \frac{i_{in}}{V_{in}} \cdot \frac{V_{out}}{i_{in}} = g_m \cdot R_{out}$

Cascode Bandwidth

- Draw in the C_{gs} and C_{gd} capacitors.
- Which ones are Miller effected?
- Is this better or worse than a CS without a CG?



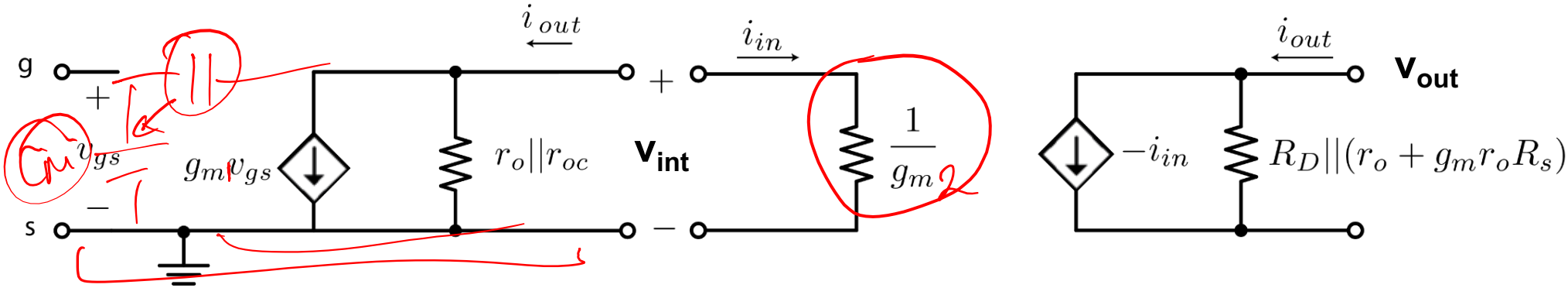
$C_M \triangleq C_{gd}(1-A)$

$C_M = C_{gd}(1-(-1))$

$\Rightarrow 2\,C_{gd}$.

Cascode Bandwidth

- **Draw in the capacitors and input resistance**



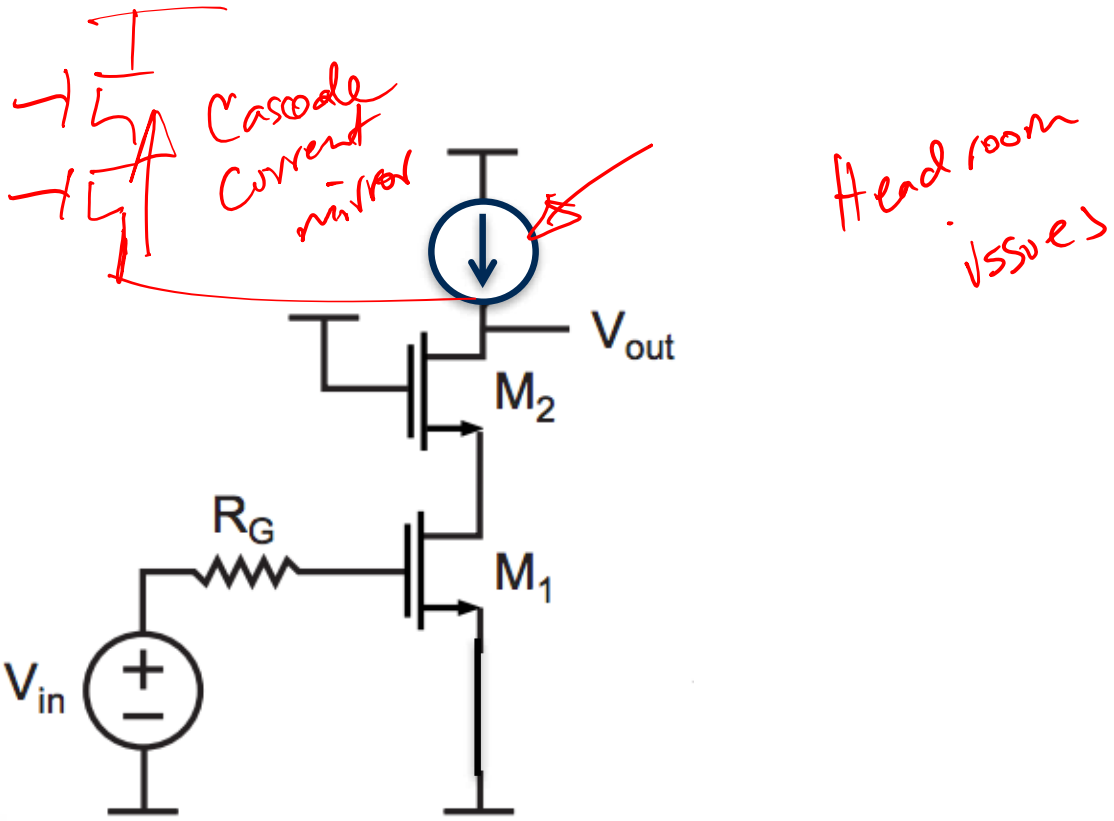
$$C_M = C_{gd}(1+A)$$

$$= C_{gd}\left(1 + g_{m1}\left(r_o \,||\, \frac{1}{g_{m2}}\right)\right)$$

$$= C_{gd}\left(1 + \frac{g_{m1}}{g_{m2}}\right) \approx \underline{\underline{2 \cdot C_{gd}}}.$$

Cascode Biasing

- CG has a very large output resistance
- Loading it with R_D is likely to reduce the voltage gain
- We can increase the gain by using a current source load, but r_{oc} needs to be very large. Can use a cascode current mirror!

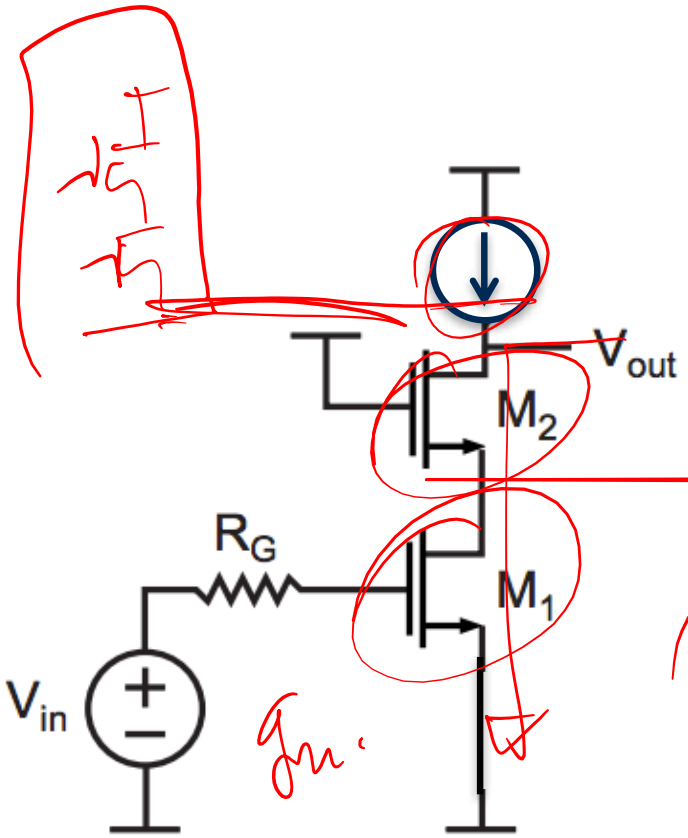


Headroom issues

Complete Amplifier Design

Goals: $g_{m1} = 1\ \text{mS}$, $R_{out} = 5\ \text{M}\Omega$

For simplicity, let's assume all g_m and r_o values are equal



$$A_V \approx -g_{m1} R_{out} = -1mS * 5M\Omega = -5{,}000$$

$$R_{out} \approx \frac{1}{2} g_m r_o^2 = 5M\Omega$$

$$r_o = \sqrt{\frac{20M\Omega}{g_m}} = \sqrt{\frac{10M\Omega}{1mS}} = 100k\Omega$$

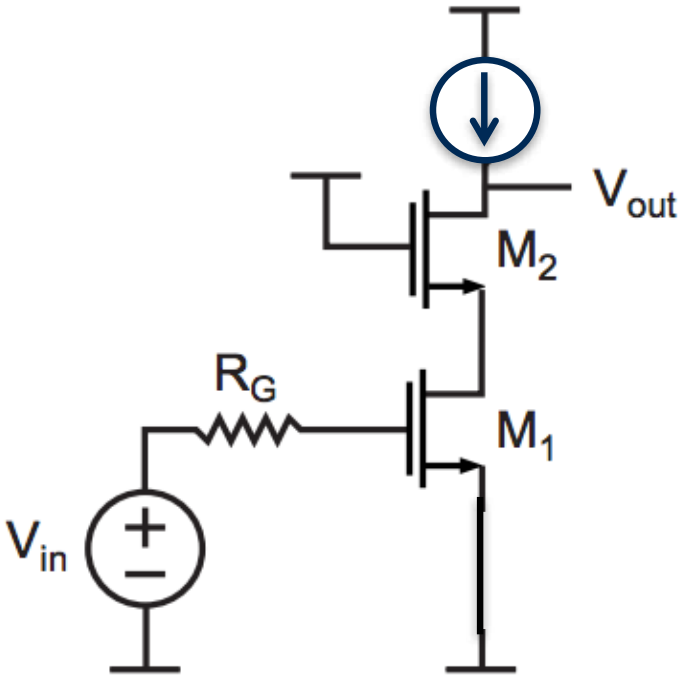
$A_V = g_{m1} \cdot R_{out} = g_{m1} \cdot g_{m2} \cdot R_{out} r_o^2$

Bias Current & Device Sizing

Need to know process parameters to solve for W/L

k' = 100 μA/V²

λ = 0.1 [V⁻¹]



$$r_o = \frac{1}{\lambda I_{DS}} = 100k\Omega$$

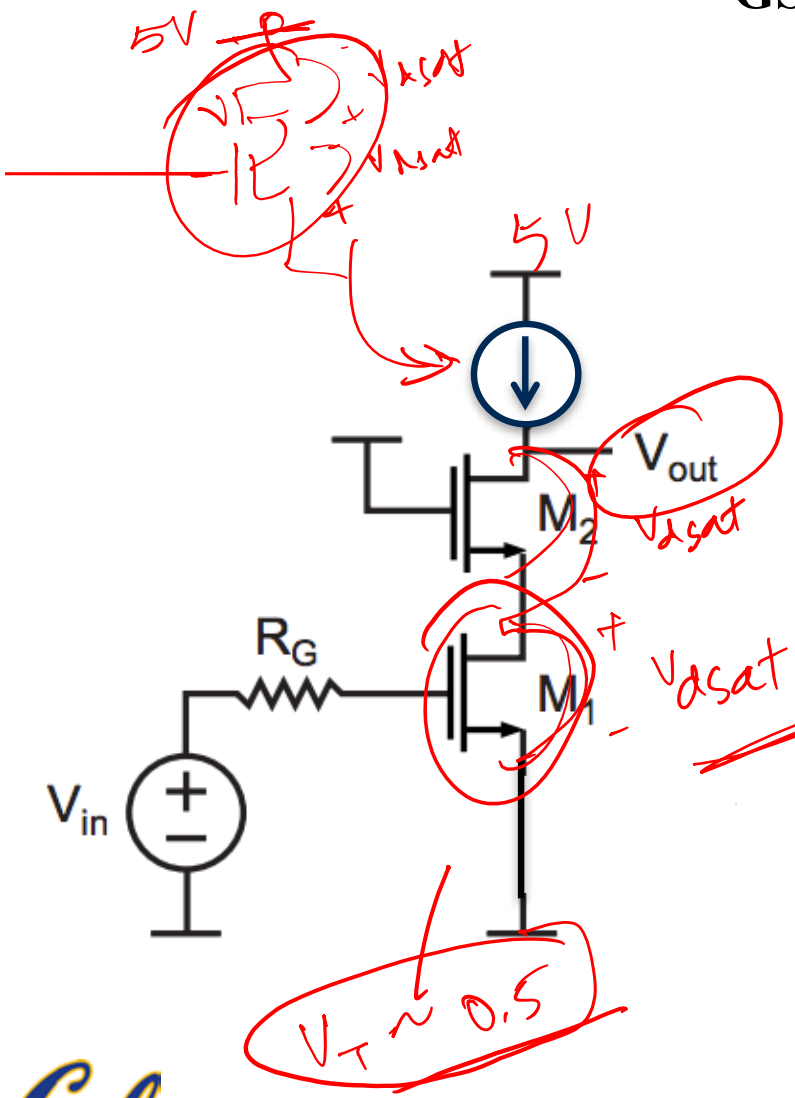
$$I_{DS} = \frac{1}{.1V^{-1} * 100k\Omega} = 100\mu A$$

$$g_m = \sqrt{2k'\left(\frac{W}{L}\right)I_{DS}} = 1mS$$

$$\frac{W}{L} = \frac{g_m^2}{2k'I_{DS}} = \frac{(1mS)^2}{2*100\mu*100\mu A} = 50$$

Output (Voltage) Swing

Need to know $V_{GS} - V_T$ (e.g. V_{DSAT}, V_{OV})



$$g_m = \frac{2I_{DS}}{V_{GS} - V_T} = 1mS$$

$$V_{GS} - V_T = \frac{2I_{DS}}{g_m} = \frac{2 * 100\mu A}{1mS} = 0.2V$$

$V_{dsat} \sim 0.2$

$V_T \sim 0.5$

$V_{GS} - V_T \sim 0.5 < V_{DS} = 0.2$

$V_{GS} < 0.7$

Maximum V_{OUT} = $V_{DD} - 2V_{dsat} = 4.6$

Minimum V_{OUT} = 0.4 V.

Input Bias V_{IN} = 0.7 V.